

ISSCC1974 Paper on Buried Channel CCD

PhD Thesis Paper by Yoshiaki Daimon Hagiwara

ISSCC 74/THURSDAY, FEBRUARY 14, 1974/COMMONWEALTH H-J BALLROOM/1:30-5:45 P.M.

Exact Dynamic BCCD Charge Transfer Analysis based on Two-dimensional Space and Time (XY and T) Numerical Computation

SESSION XIII: Charge-Coupled Devices and Applications

Chairman: Lewis M. Terman

IBM T. J. Watson Research Center, Yorktown Heights, N. Y.

THPM 13.1: Charge Transfer in Buried-Channel Charge-Coupled Devices*

Yoshiaki Daimon, Amir M. Mohsen** and Thomas C. McGill

California Institute of Technology

Pasadena, Cal.

PREVIOUS THEORETICAL work¹⁻¹² on the operation of charge transfer devices has focused upon surface charge-coupled devices and integrated circuit versions of the bucket-brigade shift registers. Another type of charge transfer device, namely buried-channel charge-coupled devices¹³, is known to have several advantages over the former two devices. However, up to the present, only a static two-dimensional model¹⁴⁻¹⁵ of buried-channel charge-coupled devices has been considered. The static model has not been incorporated in dynamic charge transfer description, and, consequently, our understanding of the device operation has been quite qualitative.

In this paper the results of a detailed numerical simulation of the charge transfer process in an overlapping gate buried channel CCD¹⁶ will be presented. The general set of partial differential equations describing charge transfer and the electrostatic potential are reduced to a set of two partial differential equations involving a single spatial dimension and the time. To accomplish this a simple capacitance network model¹⁷ has been

used to reduce the appropriate two dimensional Poisson's equation into a second-order differential equation in a single spatial dimension. The resulting equation relates the signal charge and the minimum channel potential under all the relevant electrodes and interelectrode regions. A diffusion equation describing the charge transfer is coupled to this equation. The resulting coupled differential equations have been solved numerically by a modified box scheme¹⁸.

It is shown that the charge-transfer process in buried-channel CCD devices can be divided into three distinct stages similar to surface channel; Figure 1. In the first stage, the charge is confined under the source storage gate and spreads itself according to the rapidly changing clock voltages. During the second stage, the charge transfer occurs in a manner analogous to the operation of a buried channel IGFET¹⁹. The storage electrodes act as source and drain, and the transfer electrode acts as the control gate. In the final stage, the charge transfer process is characterized by transfer induced by the relatively large fringing fields. The residual charge decays exponentially

*Supported in part by the Naval Research Laboratories under Contract No. N00014-67-A-0094-0032.

**Present Address: Bell Telephone Labs, Murray Hill, New Jersey.

¹ Kim, C. K., and Lenzlinger, M., "Charge Transfer in Charge Coupled Devices," *J. Appl. Phys.* 42, p. 3586-3594; 1971.

² Strain, R. J. and Schryer, N. L., "A Nonlinear Diffusion Analysis of Charge-Coupled Device Transfer," *B.S.T.J.* 50/No. 6, p. 1721-1740; 1971.

³ Engler, W. E., Tiemann, J. J., and Baertsch, R. D., *Applied Physics Letters* 17, p. 469; 1970.

⁴ Carnes, J. E., Kosonocky, W. F., and Ramberg, E. G., *IEEE Journal of Solid State Circuits*, p. 312-326; Oct., 1971.

⁵ Carnes, J. E., Kosonocky, W. F., and Ramberg, E. G., "Free Charge Transfer in Charge-Coupled Devices," *IEEE Transactions on Electron Devices*, p. 798-808; June, 1972.

⁶ Berglund, C. N., and Thornber, K. K., "A Fundamental Comparison of Incomplete Charge Transfer in Charge Transfer Devices," *B.S.T.J.*, 52/No. 2, p. 147-182; 1973.

⁷ Berglund, C. N. and Thornber, K. K., "Incomplete Transfer in Charge Transfer Devices," *IEEE J. of Solid State Circuits*, SC-8/No. 2; p. 108-116; 1973.

⁸ Mohsen, A. M., McGill, T. C., Daimon, Y. and Mead, C. A., "The Influence of Interface States on Incomplete Charge Transfer in Overlapping Gate Charge-Coupled Devices," *IEEE J. of Solid State Circuits*, SC-8/No. 2, p. 125-138; 1973.

⁹ Heller, L. G., and Lee, Hsing-San, "Digital Signal Transfer in Charge-Transfer Devices," *IEEE J. of Solid State Circuits*, SC-8/No. 2, p. 116-125; 1973.

¹⁰ Mohsen, A. M., McGill, T. C., and Mead, C. A., "Charge Transfer in Overlapping Gates Charge Coupled Devices," *J. of Solid State Circuit*, SC-8/No. 3, p. 191-207; 1973.

¹¹ Daimon, Y., Mohsen, A. M., and McGill, T. C., "Final Stage of the Charge Transfer Process in Charge Coupled Devices," *IEEE Transactions on Electron Devices*; to be published.

¹² Thornber, K. K., "Incomplete Charge Transfer in IGFET Bucket-Brigade Shift Registers," *IEEE Transactions on Electron Devices*, Vol. ED-18/No. 10; Oct., 1971.

¹³ Walden, R. H., Krambeck, R. H., Strain, R. J., McKenna, J. N. L., and Smith, G. E., "The Buried Channel Charge Coupled Devices," *B.S.T.J.*, p. 1635-1640; Sept., 1972.

¹⁴ McKenna, J., and Schryer, N. L., "The Potential in a Charge Coupled Device with No Mobility Carriers and Zero Plate Separation," *B.S.T.J.*, 52/No. 5, p. 669-696; 1973.

¹⁵ Kent, W. H., "Charge Distribution in Buried Channel Charge Coupled Devices," *B.S.T.J.* 52/No. 6, p. 1009-1024; 1973.

¹⁶ Mohsen, A. M., McGill, T. C., and Zimmerman, T., *Electronics Letters*, p. 396-398; Aug., 1973.

¹⁷ Daimon, Y., and McGill, T. C., "Electrostatic Analysis of Buried Channel Charge Coupled Devices," *Transactions on Electron Devices*; to be published.

¹⁸ Keller, H. B., "Numerical Solution of Partial Differential Equations," *Academic Press*, p. 327; 1971.

¹⁹ Daimon, Y., and McGill, T. C., "Buried Channel Charge Transfer Devices," *Transactions on Electron Devices*; to be published.

ISSCC1974 Paper on Buried Channel CCD

PhD Thesis Paper by Yoshiaki Daimon Hagiwara

ISSCC 74/THURSDAY, FEBRUARY 14, 1974/COMMONWEALTH H-J BALLROOM/THPM 13.1

with a final characteristic time constant of the order of a nanosecond; Figure 2¹¹.

In light of these reliable numerical results, the entire charge transfer process has been reviewed analytically. Approximate analytic expressions for the charge-transfer efficiency which are sufficiently accurate to be used in optimizing CCD array design with respect to voltage waveform and clocking scheme will be presented.

The numerical results for the charge transfer in the buried channel CCD are presented as a motion picture which illustrates graphically the distinct features in the operation of a buried channel CCD, under several clocking schemes.

Figure 1(a) plots the minimum potential, charge profile and current density at $t = 0.221$ ns. At $t = 0$, the transfer and drain gate voltages start dropping to the final value (-12 V) from the initial value (8 V). The plot is shown at the gate voltages of -10 V. The barrier and source gate voltages are set to be 8 V throughout the transfer process.

Charge is normalized by 935 electron charges/ μ^2 . Sheet current density is normalized by 23.4 electron charges/ $\mu \cdot \text{ns}$. The length L of one unit cell of the device is 48μ consisting of two polysilicon gates and two aluminum gates.

In Figure 1(b), $t = 0.443$ ns. Note the current density under the transfer gate is almost constant. The charge transfer in this stage can be described quite accurately by buried channel IGFET¹⁹.

In Figure 1(c), $t = 1.05$ ns. Note the slope of the current density indicates that the net charge under the transfer gate is still decreasing. The charge transfer in this final stage is characterized by the powerful field-aided transfer¹¹.

In Figure 2 (top), sheet current density is normalized by 23.4 electron charges/ $\mu \cdot \text{ns}$. Time is normalized by $t = (0.001) L^2/D = 1.92$ ns with $L = 48 \mu$ and $D = 12 \text{ cm}^2/\text{s}$. The lines (a), (b), and (c) present the net charging, charging and discharging of the transfer gates, respectively.

In Figure 2 (bottom), charge is shown as a percentage of the total signal charge of 45,000 electron charges/ μ . The lines (a), (b), and (c) represent the total residual charge under the source and transfer gates, the charge under the source gate, and the charge under the transfer gate respectively. Note the lines eventually become straight, implying the exponential decay characteristics of the powerful field-aided transfer. The final slope (hence, the characteristic time constant) is 0.765 ns for lines (a) and (c), and 0.165 ns for line (b).

Exact Dynamic BCCD Charge Transfer Analysis based on Two-dimensional Space and Time (XY and T) Numerical Computation

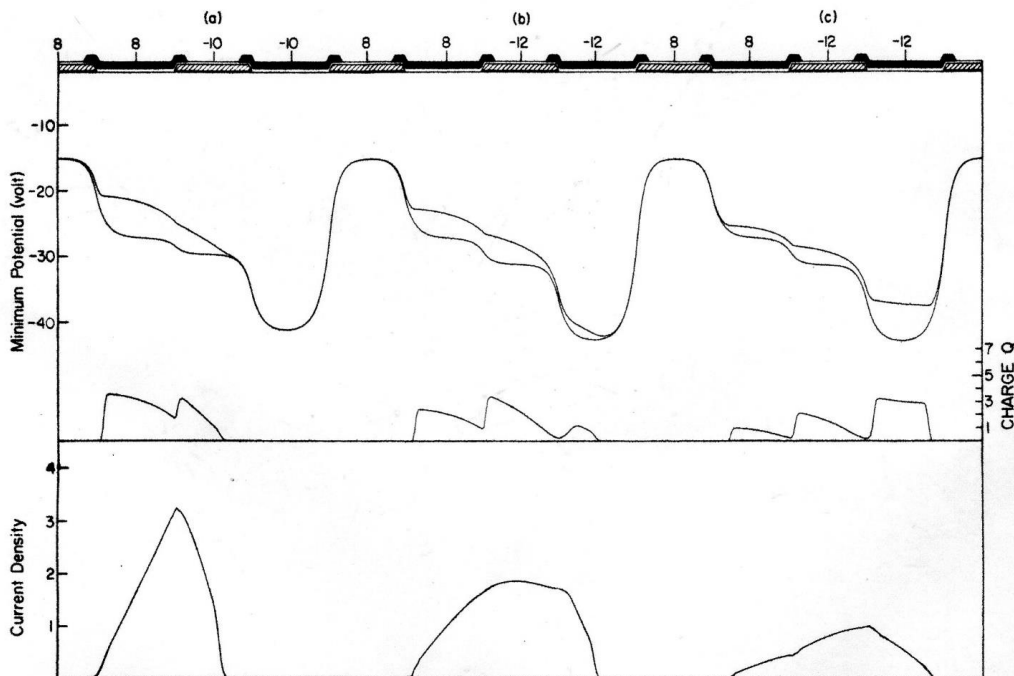
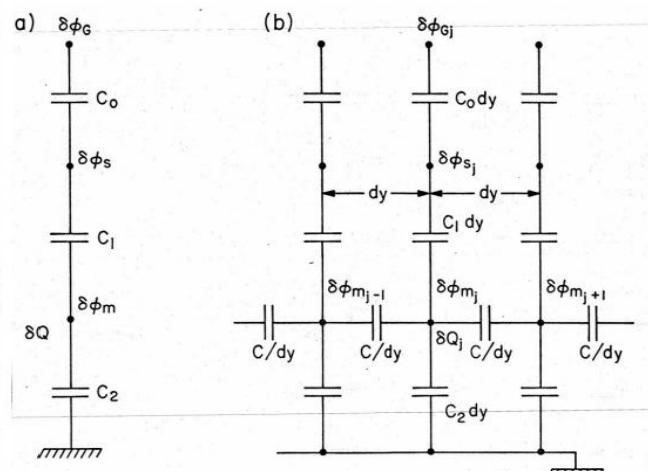


FIGURE 1—Plots of the minimum potential; charge profile and current density at different stages of the charge transfer.

[See page 245 for Figure 2.]

Charge Transfer in Buried-Channel Charge-Coupled Devices
(Continued from Page 147)



The capacitance network for one dimensional MOS structure (a) and two dimensional structure (b)